ABSTRAT OF THE DISCLOSURE

A scan test circuit is provided with a scan chain having n pieces of scan storage elements (n: integer, n>1); a scan clock generation circuit which is able to control a frequency of a first clock to be used for shifting data into the first to (n-1)th scan storage elements, and a frequency of a second clock to be used for shifting data into the n-th scan storage element and performing actual operation, independently from each other; and a scan selection internal signal generation circuit for generating a scan selection internal signal that is synchronized with the second clock.